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@HDL RELEASES ASSERTION-BASED VERIFICATION

SUPPORT FOR ACCELLERA PSL SUGAR LANGUAGE

**Newest Versions of @Verifier and @Designer Products Deliver
Full Interoperability with Cadence NC-Sim LDV 4.1**

SAN JOSE, CALIFORNIA – January 24, 2003 - @HDL, Incorporated, a leading vendor of electronic design automation for accelerating functional verification, today announced the release of its @Verifier and @Designer 3.0 products with full support of the Accellera PSL Sugar 2.0 language. The assertion-based verification and debugging capabilities available in @Verifier and @Designer deliver full interoperability with the newest release of the Cadence NC-Sim logic simulation product, LDV 4.1, which adds direct simulation support for the PSL Sugar 2.0 assertion language. @HDL will be demonstrating the @Verifier and @Designer software running with NC-Sim at industry trade shows next week in California and Japan.

"@HDL has implemented support for Sugar 2.0 in their @Verifier and @Designer products within an impressively short time frame. They've have done an excellent job in language support and in ensuring tool interoperability. With its comprehensive support of Sugar in both simulation and model checking flows, their @Verifier product will enable design verification teams to immediately incorporate Sugar into their development environments," stated Dr. Yaron Wolfsthal, manager of formal methods at IBM's Haifa, Israel, research lab, where the Sugar language was conceived.

"We've run @HDL tools on several multi-million gate ASIC designs and have found substantial value in working with our customers to help them filter out problems earlier in the ASIC design cycle" stated Jamshed Qamar, vice president of ASIC Business Development and Engineering, Oki Semiconductor. "We have also started to evaluate the enhanced capabilities of the @HDL tools, which include tighter integration with NC-Sim and automatically extracted assertions in the Sugar format, for IP integration verification."

"Assertion-based verification allows chip development teams to eliminate functional errors much earlier in the design process. @HDL has been working closely

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with Cadence to ensure full interoperability with the newest release of NC-Sim, which incorporates support for Sugar,” stated Tarak Parikh, vice president of product engineering for @HDL. “Rapid adoption of assertion-based verification using Sugar will happen as our customers see smooth and effective interoperability between NC-Sim and our @Verifier and @Designer products. We look forward to working co-operatively with Cadence to allow rapid adoption and deployment of Sugar assertion-based verification in the SoC design community.”

@Verifier 3.0 and @Designer 3.0 with Sugar Support

***** Check out the DVCon 2003 Presentation by @HDL**

www.athdl.com/pdf/pulsugar.pdf

Both @Verifier 3.0 and @Designer 3.0 are available immediately, running on Linux and Sun/Solaris workstations. Licenses are available for both time-based and perpetual use.

@Verifier automatically extracts properties from RTL designs to uncover such problems as multiple clock domain synchronization errors, Finite State Machine (FSM) deadlock, and code reach-ability errors. These automatically extracted properties are also output as Sugar assertions, which can be run directly in NC-Sim simulation, thereby utilizing the existing System-on-Chip (SoC) test benches to uncover other, difficult to find, functional errors. In addition, designers can write their system-level assertions and properties using Sugar 2.0 assertions. These assertions are then run through the formal model checking engines incorporated in @Verifier. The @Verifier-DP product, offering automatic, distributed processing for model checking, delivers even further productivity gains by running the Sugar assertions on different machines or processors in parallel. The overall model checking run times can therefore be reduced by almost a linear rate.

@Designer delivers a next generation graphical debugging and design analysis environment to quickly isolate functional errors during creation, formal model checking, and simulation of Verilog-based designs. Powerful debugging features have been added to allow a unified assertion-based verification and coverage analysis environment for Sugar assertions, with support for analysis of both NC-Sim simulation and @Verifier model checking. Extensive capabilities for debugging RTL, test benches and Sugar assertion coverage and reports are now available for use by design and verification personnel utilizing the Cadence NC-Sim LDV 4.1 simulator.

About Accellera PSL / Sugar

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Accellera is an electronic design automation (EDA) organization focused on language-based electronic design standards. Accellera's mission is to drive worldwide development and use of standards required by systems, semiconductor and design tools companies, which enhance a language-based design automation process. The Accellera Property Specification Language, PSL, based on the Sugar Assertion language, allows designers to embed information into their designs to facilitate verification. The assertion language enables the design to capture assumptions and partial specifications regarding the operation of a design in a succinct, formal and unambiguous manner.

Upcoming Exhibitions

@HDL will be exhibiting the @Verifier and @Designer products at two upcoming tradeshow in California and Japan; at the DesignCon 2003, www.designcon.com, Santa Clara Convention Center, California, January 28 and 29, at booth #101, and at the Electronic Design and Solution Fair, www.edsfair.com, Yokohama, Japan, January 30 and 31, at the Innotech booth, #207.

About @HDL

@HDL is a privately-held electronic design automation (EDA) company focused on accelerating functional verification of SoC and silicon IP designs. The @Verifier and @Designer products deliver significant verification productivity improvement for it's customers, including such companies as AMD, Fujitsu, MegaChips and Toshiba, through system-level design analysis and debugging, automatic formal model checking, and tight integration with existing Verilog simulation environments. With support of industry standard assertion languages, including OpenVera Assertions (OVA) and the Accellera PSL Sugar language, @HDL enables design teams to reap immediate productivity gains in their System-on-Chip (SoC) verification. @HDL is a member of the Cadence (NYSE: CDN) Connections Program and the Synopsys (NASDAQ: SNPS) in-Sync Program. For more information, call (408) 441-1317, visit www.atHDL.com or email to info@atHDL.com.

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